28 GHz Front –End with Duplexer in 40 nm CMOS Technology for 5G Beam-steering Transceivers

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***Abstract*— This paper presents a (transceiver) TRX front-end structure design for Phased Array applications in 40nm CMOS Bulk process. The proposed structure consists of the Power Amplifier (PA) the Low Noise Amplifier (LNA) along with a monolithic transformer duplexer for Antenna connection applied in half-duplex systems. The front end covers the millimeter wave (MMW) 5G band. The PA design contains two differential cascode stages with capacitor neutralization technique achieving a small signal gain (S_{21}) of 22.86dB with a -3dB bandwidth (BW) at 22-34 GHz. Moreover, the PA reaches a PAE_{max} of 31.66% and a P_{sat} of 18.5 dBm. The LNA design consist of two cascode stages using current reuse technique at the first stage, obtaining 17.5 dB gain (S_{21}) with a -3 dB bandwidth from 22.5 to 31 GHz. Both amplifiers are connected to the antenna through a compact duplexer with minimum losses and sufficient isolation.**

Keywords*— Low Noise Amplifier, Power Amplifier, 5G, Phased Array, Duplexer, RF front-end,current reuse, capacitor neutralization, 40 nm CMOS Technology.

I. INTRODUCTION

The majority of 5G applications require massive multiple-input, multiple-output (MIMO) performance. Thus, phased array and beam-forming systems consist the cornerstone of the 5G telecommunications.

Antennas systems in 5G have to be able to create multiple independent beams simultaneously or to be able to steer the antenna pattern at any formation and direction. The only way to achieve those requirements, is by controlling the antennas through a RF-front-end which provides wide azimuthal coverage (360º), high gain and adequate linearity. The continuously increasing demand of fully operated receivers (RX) and transmitters (TX) in 5G frequencies from 24.25 GHz to 29.5 GHz renders the design of RF-front-ends extremely challenging.

CMOS technology with the increase of the cut off frequency has achieved high performance on mm-wave frequencies. As a result, fully integrated front-ends for phased array and beam forming systems, are developed. Such front-end architectures, as the illustrated in the Fig.1, are able to present high, controllable gain through PA, LNA and VGA (Variable Gain Amplifier) circuits and a 360º phase control using Phase Shifters (PSs) in receiver and transmitter chain.

In recent years there have been many studies regarding phased array systems either employing full duplex [1] or half-duplex communication [2]. Both pose advantages and disadvantages for 5G millimeter wave communication, although they require different approach in the design. The half-duplex communication allows only one chain TX or RX to be functional at a time demanding the design of high isolation and efficient switching structures between the two chains [3]. However, most front ends in the literature, that provide satisfactory performance focus on smaller bands of the MMW 5G rather than the entire spectrum [4] [5] [6]. This tendency is due to the considerable challenges in designing wideband MMW power and low noise amplifiers covering the overall 5G band especially in CMOS process [7], [8]. Furthermore, extensive work has been published on the connection of the TX and RX chains to the antenna. Most proposed systems separate matching networks for the PA and LNA [9], while other works implement the connection with the antenna by designing duplexer structures which combine the TX/RX chain at one multi-spiral transformer in a more compact and chip area saving way [10].

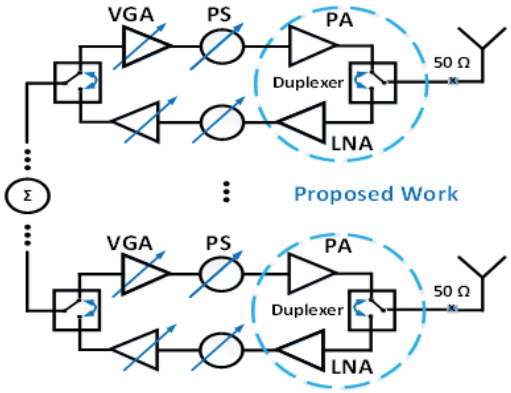

Fig. 1. Simplified diagram of the proposed front-end.

Taking into account the aforementioned front-end design issues and challenges, a front end topology is proposed which contains the PA and LNA circuits alongside with the design of a duplexer-transformer before the antenna. This work presents the design of the PA, LNA and duplexer which constitute the most critical elements of the MMW front-end. The proposed circuits cover efficiently the overall 5G band while occupying minimum chip area. The PA consists of differential stages interconnected through transformers while the LNA employs two stages with current reuse technique to compensate for gain losses. Furthermore, a novel design and layout for an efficient antenna duplexer is presented.

In Section II the proposed PA and LNA designs are presented. Additionally, in Section II the monolithic duplexer is described along with its characteristics. The Section III covers the overall performance of the proposed work where simulations results are illustrated. Finally, the conclusion, acknowledgement and references are presented in Section IV.

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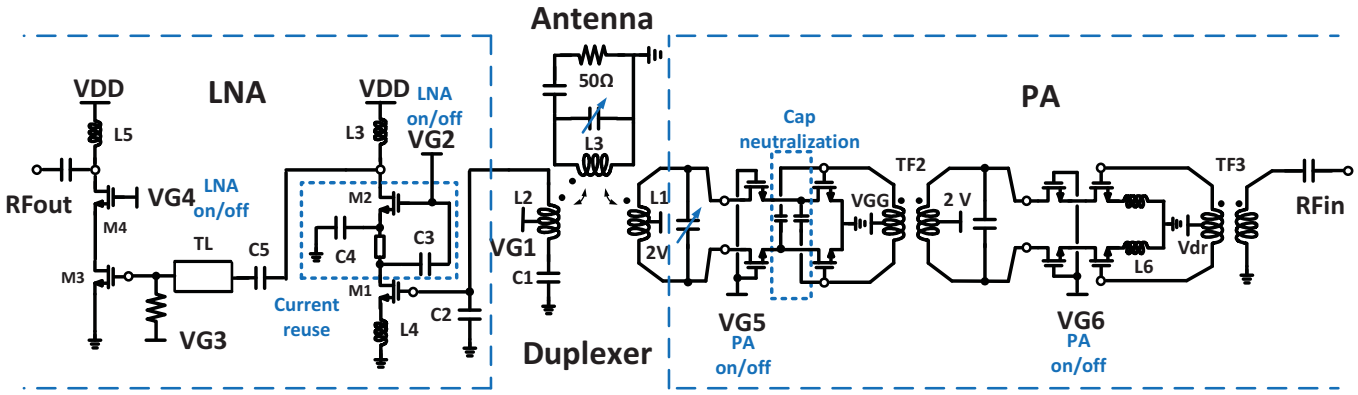

Fig. 2. Schematic diagram of proposed front end

II. CIRCUIT DESCRIPTION

A. Low Noise Amplifier Design

The proposed LNA topology consists of two stages as it is illustrated in Fig. 2 (left side). Although both stages are cascode topologies they present different design characteristics. In the first stage, the transistor M_1, the Common Source (CS) part of the cascode configuration, is designed with adequate width to satisfy the bandwidth needs of the font-end. In this way, the gain requirements of full 5G band from 24.25 to 29.5GHz are fulfilled. The CS part is combined with a Common Gate (CG) amplifier in order to compose the cascode configuration. Transistor M_2 of the CG is designed to alleviate the Miller Effect and to provide improvement of the reverse isolation (S_{12}) and stability. The Gate Voltage (V_{G1}) of the M1 transistor is fixed at 550mV for better NF performance and the voltage at the gate of M_2 is at 1.1V as the value of V_{DD}. Both gate voltages are reduced to 0V for the purpose of letting the amplifier to power down, when the PA is active. At the first stage the input matching is achieved with the L_2 inductor of the duplexer combined with the C_1 and C_2 capacitors. Moreover, for better performance in linearity and implementing the input matching, degeneration inductor (L_4) is used. The LNA presents respectable input matching from 20 to 30.5GHz (S_{11} lower than -10 dB). The drawback of the degeneration inductor is that the gain is reduced. To mitigate the gain losses at the first stage a current reuse technique is applied [11]. The current reuse technique requires the usage of two capacitors C_3 and C_4. In this case transistor M_2 of the CG acts as a pseudo-CS transistor because of the signal path to its gate created from C_3 and the AC ground path created by C_4. In this way, extra gain is obtained without further deterioration of the power consumption or of the NF. The total current drained from the first stage is 9mA.

The second stage is also in a cascode configuration. However, the design purpose of the second stage is not to achieve wide bandwidth but to amplify the gain sufficiently for the upcoming Phase Shifter where losses are projected to be caused. The interconnection between the two stages is accomplished through a transmission line. The total current drained is 4mA and the V_{DD} is at 1.1V too. The V_{G3} is stable at 450mV and the V_{G4} at 1.1V. Both voltages are turned off when the PA is in operation.

B. Power Amplifier Design

The goal of the power amplifier in this front-end design is to achieve a satisfactory power performance across all frequencies inside 5G millimeter wave spectrum. The input of the PA is matched at 50Ohm and it is load matched at the output. It consists of two differential stages cascaded together using transformer networks. Fig. 2 (right side) shows the schematic diagram of the PA chain. Both driver and final PA cells follow cascode differential topology in order to provide high output power, isolation, gain, stability and wide bandwidth. In addition, the power performance limit, due to breakdown voltage of the device, is overcome by the cascode topology allowing for a supply voltage of $2xV_{DD}$. In the design the supply of both driver and final PA is chosen to be at 2V, a little lower than the mentioned theoretical value, in order to ensure safe functionality over all PVT variations. The size and bias of both stages are chosen after extensive parametric load pull simulations. Inside the final PA cell, the capacitor neutralization technique is implemented, providing reverse isolation, increase of the stability factor K and power gain [12]. The cross capacitor connects the gate of the CS +device to the drain of the CS –device and vice versa forming a capacitance that neutralizes the parasitic capacitance C_{gd} of the device. In the driver stage no capacitor neutralization technique is used, while in order to perform wideband input matching, a degeneration inductor is used (L_6) with an inductance of 57pH. This inductor increases the real part of the input impedance without degrading significantly the power performance. In this design three transformer structures have been created at the input, inter-stage and output. Firstly, the output transformer is designed to provide load matching with equal power performance inside the overall 5G spectrum. A capacitor is placed in parallel with the primary of the output transformer for tuning purposes. More details about the output transformer windings will be given in the section of the duplexer. Apart from the output transformer, an inter-stage 2:1 transformer has been designed to connect the two stages efficiently. The quality factor of its windings is high so as not to suffer additional losses, while the coupling factor between the windings is low to provide the needed interstage matching across the entire bandwidth. The input matching is achieved through a 1:1 low coupling transformer and the degeneration inductor. Those two passive components must present as low coupling as possible between them, otherwise the impedance matching cannot be achieved regardless the value of the L_6.

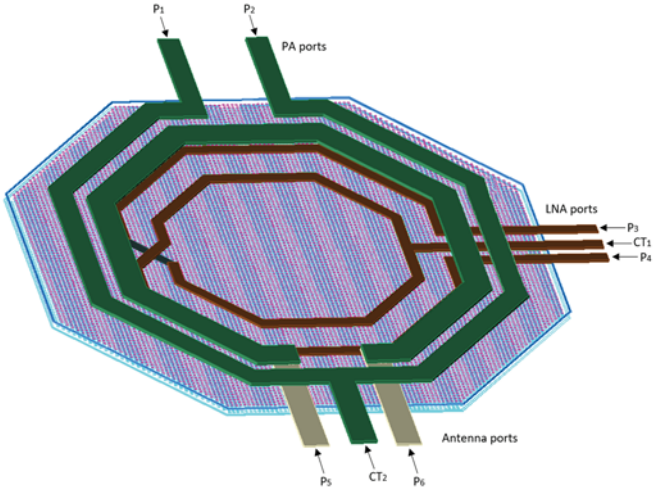

Fig. 3. Monolithic duplexer layout diagram

TABLE1. Duplexer's Inductors and Characteristics

Inductors	Inductance (pH)	Quality Factor	Input Loss (dB)
L1 (PA)	432	14.1	-1.65
L2 (LNA)	387	4.6	-2.37
L3 (Antenna)	335	8.9	-2.85

C. Monolithic duplexer design

The TX, RX chains are connected to the antenna through a duplexer (Fig. 2) which couples electromagnetically the signals from PA to antenna for transmission and from antenna to LNA for reception. Such duplexers have only recently been introduced. The proposed duplexer exhibits a very wide bandwidth and provides a compact solution for half duplex systems saving a lot of chip area. However, for an efficient duplex design low input losses are needed at all connected ports and high isolation between LNA and PA. In this topology, three windings have been used: the PA inductor is coupled through a planar topology with the antenna while the LNA winding is stacked below the antenna.

Initially, the antenna inductor (L_3) presents inductance of 335pH and is designed with the purpose of providing adequate electromagnetic coupling between L_3 and the front-end inductors (L_1, L_2). The design of the PA output inductor requires high quality factor to minimize losses. The LNA input inductor demands low input losses (for low NF), and quality factor in order to facilitate the input matching for wideband performance. This method provides a compact solution saving a lot of chip area.

The construction of the duplexer is accomplished using copper layers M6 to M8 and the aluminum layer AP of the TSMC 40nm CMOS technology. The antenna and the PA windings are designed on AP layer with the antenna winding placed in the interior of the PA inductor. The LNA inductor consist of a two-spiral structure on M7 layer for achieving lower Q and reduced coupling with the PA inductor. The coupling coefficient factor between LNA and PA is 0.3 and the isolation between them reaches -14.9dB. The diameter of duplexer is 235um with guard-ring and 203um without. Finally, the metal widths of the windings are chosen to withstand the produced currents from the PA under possible PVT variations.

III. SIMULATION RESULTS

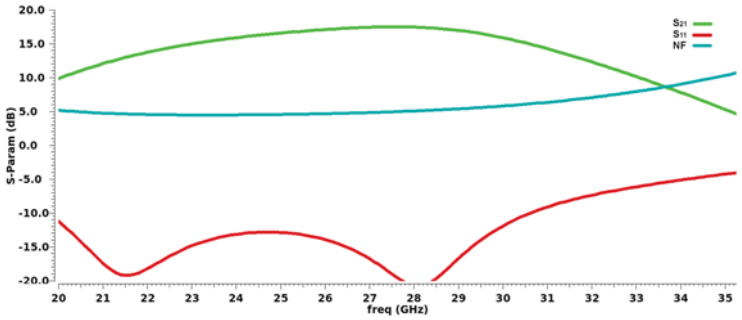

Fig. 4. S-parameters simulations of the LNA combined with the duplexer

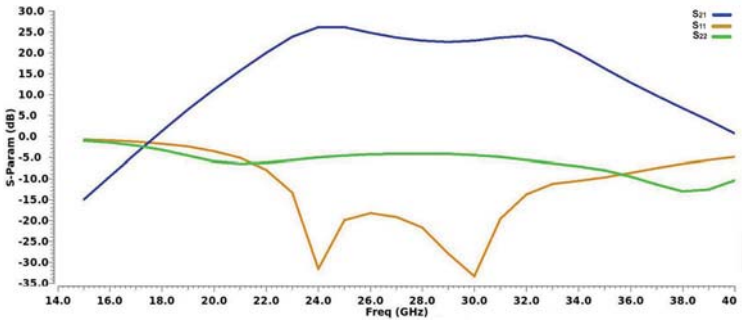

Fig. 5. S-parameters simulations of the PA combined with the duplexer

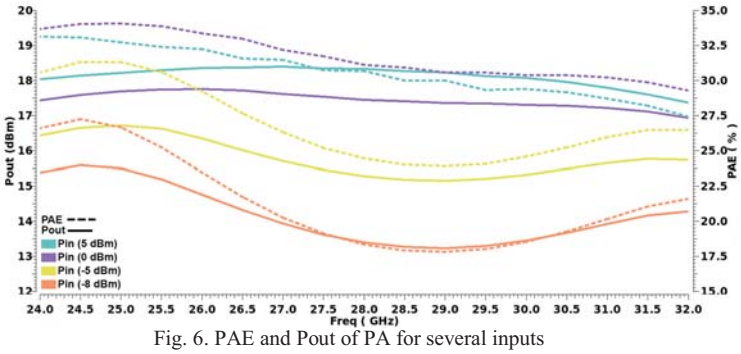

Fig. 6. PAE and Pout of PA for several inputs

The proposed LNA, PA circuits and the duplexer are designed in 40nm CMOS Bulk technology and simulated in the environment of Cadence software. The duplexer, along with the PA's transformers and the interconnect paths of the LNA are EM simulated with the ADS Momentum software.

The S-parameters of the two-stage LNA are presented at Fig.4. The gain (S_{21}) of the amplifier is 17.5dB with a -3 dB bandwidth from 22.5 to 31GHz with 4.5dB NF. The achieved input matching ranges from 20-30.5GHz. The entire power consumption of the two stages is 14.3mW and unconditional stability is secured.

In Fig. 5 the small signal analysis of the PA is depicted. The PA achieves a S_{21} of 22.81dB at 28 GHz with a 3 dB bandwidth of 12 GHz and a S_{11} lower than -10 dB from 22.4-34 GHz. Under large signal operation the PA exhibits a constant behavior across the 24GHz to 32GHz frequency range (Fig. 6) while delivering saturation power of 18.5 dBm and a peak PAE of 31.66% at 28GHz. Also, at P1dB of 9.4dBm it produces a power output level of 12.41 dBm and a PAE of 15.41 %. Finally, the power consumption of the PA is 91mW.

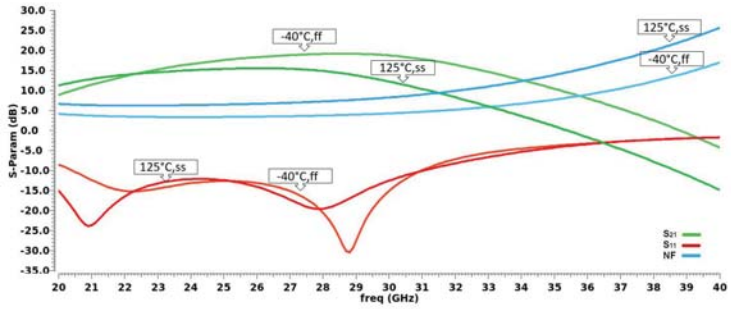

Fig. 7. LNA corner S-parameter simulation for -40oC/ff and 125oC/ss

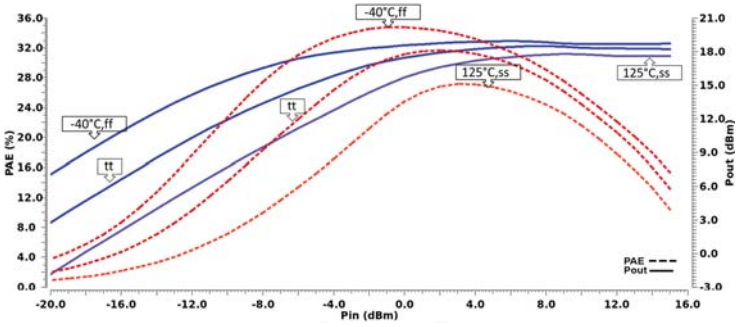

Fig. 8. PA PAE and output power corner simulations at 28 GHz.

In order to evaluate the performance of the proposed front-end design, simulation considering PT (process-temperature) variations, are performed. More specifically, Fig. 7,8 present the S-parameter and large signal analysis of LNA and PA respectively under the worst-case scenarios of process and temperature. The slow-slow (ss) and fast-fast (ff) device variations are chosen to be presented along with the lowest and highest temperature determined by the technology.

The LNA corner variations are illustrated at Fig 7. is illustrated These are the -40ºC combined with the ff process and the 125ºC combined with the ss in order to evaluate the highest and the lowest possible gain behaviors respectively. As is noticed from t Fig. 7, the LNA preserves the desirable bandwidth and maintains the input matching at both cases. Furthermore, in Fig.8 the PA is stressed under the same conditions at 28 GHz providing acceptable performance for both output power and PAE. The output power deviates equally from the typical condition by a maximum of 5 dBm at each worst scenario, while the PAE varies by a maximum of 9%.

CONCLUSION

This paper presents a front-end design topology for beam-steering half duplex applications. The structure consists of the LNA and the PA which are specifically designed to completely cover the overall MMW 5G spectrum. The connection of the front-end chain with the antenna is realized through the utilization of a very wide bandwidth, compact, low loss, high isolation duplexer-transformer, enabling the development and implementation of chip area efficient and high-performance parallel channels for beam-steering systems.

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